ASIC Design Essentials

Synopsis

This course is aimed to provide an opportunity for the participant to acquire technical and business insight into some of the vital aspects of ASIC design. As most of these aspects also hold true for general IC design, this course will also greatly benefit an IC Design Engineer.

Application Specific Integrated Circuit (ASIC) is a major topic of interest in the highly competitive field of VLSI circuits where each industry player tries to outdo the other by introducing a niche and differentiated product ahead of the competition. While products assembled from off-the-shelf components are faster to reach the market, they ride on an already existing product wave. With ASICs, however, one can be the forerunner and tap into the initial and major chunk of the market window grossing high revenues. The exclusive design rights also provide an added advantage.

This course is aimed to provide useful insight into some of the vital issues seen in sub micron designs. It also throws light on some emerging trends. It will enable your Design Engineer to understand some of the basics involved in various phases of the ASIC development chain, from A Request for Quote to Working Silicon, with an appreciation of how activities and decisions made in one phase affects another. It will also enable your Customer Support Engineering staff to provide an effective and proactive support to your customer. This course also provides a well-structured guideline to Business Development Engineers.

The course is structured into modules. Short interactive workshops within the course facilitate in making this an interesting, interactive learning experience. Participants will be exposed to issues cited from real industry experience.

This course will be delivered by a senior VLSI consultant with extensive exposure in supporting & managing ASIC projects on a global scale.

What You Will Learn

- Basics of ASIC Design Libraries, Design Flow
- Basics of Design for Re-use and IPs
- Guidelines for Low Power design
- Basics of Verification especially DFM/DFY
- Insight into ASIC technology and market trends
- Overview of MPW/MRS
- These in turn will enable you in
  - How to effectively communicate with your customers
  - How to effectively support your customers

Who Should Attend

- General IC & ASIC Design Engineers (fresh or with 1-2 years experience)
- Product Development Engineers
- Customer Support Engineers
- Business Development Professionals

Prerequisite

Basic engineering know how. 1-2 years experience in IC design/support is preferable.

Course Methodology

This course is conducted in English and in a seminar room. The course will include brief interactive workshops like sessions to encourage participation and facilitate learning. Each participant will receive a set of course material.

Course Duration

2 days, 9:00am – 5 pm
This is an abridged version of the actual course, "ASICs – Concept to Product". The latter is a 3 days course

Course Structure

The course is organized into modules to facilitate participants to attend a specific module(s) as per their interest/need. To extract maximum benefit from the course however, participation in all modules is recommended.

DAY 1

A. Introduction to ASICs

i. Standard cell based ASIC
ii. Semi custom ASIC and Full custom ASIC
iii. Brief outline of Design Flow
iv. Brief outline of Library

B. Design Library

i. Definition
ii. Library Architecture
(with basic introduction to SSIs, IOs, Memories, IPs; general circuits used like Flip flops, latches, combinational circuits, RAMs, ROMs etc. will be included)
iii. Library Cell Representations
iv. Cell views (logical description, timing information, derating data, capacitance information, power and area information)
v. Global views (max capacitance, interconnect info, max power and derating information)
vi. Library Characterization
Standard load, trip points, parasitic caps, input slew rate, timing equation (predicting delay), example of predicting delay
vii. Library Validation
viii. Trends in Library architecture
Power, speed optimization, drive, contents changing with technology and trends

C. Verification, DFT and DFM

i. Need
ii. Functional Verification
    a. Simulation
    b. Formal Verification
    c. Code coverage
    d. Assertion Based Verification
    e. Analog Mixed Signal
iii. Timing Verification
    a. STA
    b. SSTA
iv. DFT
    a. Scan
        1. Full scan
        2. Boundary scan
    b. Faults – Fault models, Fault collapsing, IDDQ test, Fault simulation
    c. ATPG
    d. At speed Testing
    e. BIST
    f. Test logic insertion
v. Physical Verification
    a. DRC
    b. LVS
    c. Parasitic Extraction
vi. Design for Manufacturability/Design for Yield (DFM/DFY)

D. Multi Project Wafer Service/Multi Reticle Service

i. What is MPW
ii. When to/Why/Who goes for MPW
iii. Generic MPW Flow model
iv. What is Multi Reticle Service
v. Foundry Perspective
(Project Scheduling, Capacity Planning, General Pricing considerations)

DAY 2

E. Low Power Design Guidelines

i. Sources of power dissipation
ii. Low power design techniques and methodologies (levels of low power optimization)
iii. Low power design tools classification
iv. Guidelines for low power design

F. Design for Re-use & IPs

i. What is IP, what is Design Re-use
ii. IPs (Driving factors, IP selection, IP verification, issues involved, generic portfolio)
iii. Concurrently developed in-house IPs
iv. Practical Design Re-use approach and essentials
v. IP market landscape
vi. Industry bodies

G. Trends in the ASIC market

i. Some definitions
ii. Shift in ASIC technology & the underlying reasons
iii. Insight into Structured ASICs/Platform ASICs
   a. IPs used in Platform ASIC
   b. Cell based ASIC vs. Platform ASIC
   c. Some industry examples illustrating the trend

Course Instructor

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Mrs. Meenu Sarin is a microelectronics professional with over 18 years experience in the microelectronics industry across various facets of operations & across geographies like Europe, India, Singapore, Greater China and Australia and with special focus in the semi custom ASIC environment. She has registered her company, VLSI Consultancy, in Singapore from which she works as a free-lance consultant. She has conducted training courses and public workshops in various countries besides delivering talks in universities. She is also a Board Member of the Microelectronics IC & System Design Association (Singapore).

From 1997-2002, Meenu was a Technical Marketing Manager in STMicroelectronics (STM)/Singapore with focus on Telecom segment. In this role, she was responsible for Business Development and Program Management for STM's semi custom ASIC projects in Asia Pacific. Meenu also worked as a Program Manager in charge of managing various semi custom projects with customers in the Asia-Pacific Region. Before her move to STM Singapore, Meenu worked at STM India from 1991 to 1997. As a Design Manager for Library Design Group, she was responsible for managing a 30 member team involved in design and development of semi custom digital libraries in various technologies across different platforms as per the market requirements and to support designers in STM's world wide locations. Prior to this, Meenu had been a Design Engineer for digital library design and development at STM Italy for several years after she received her engineering degree (Computer Engineering) from Delhi Institute of Technology, India in 1988.