



# ASICs – Concept to Product

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## Synopsis

This course is aimed to provide an opportunity for the participant to acquire comprehensive technical and business insight into the ASIC world. As most of these aspects also hold true for general IC design, this course will also greatly benefit an IC Design Engineer.

Application Specific Integrated Circuit (ASIC) is a major topic of interest in the highly competitive field of VLSI circuits where each industry player tries to outdo the other by introducing a niche and differentiated product ahead of the competition. While products assembled from off-the-shelf components are faster to reach the market, they ride on an already existing product wave. With ASICs, however, one can be the forerunner and tap into the initial and major chunk of the market window grossing high revenues. The exclusive design rights also provide an added advantage.

This course is aimed to provide a basic understanding of the ASIC development chain. It will enable your Design Engineer to understand the basics involved in various phases of the ASIC development chain, from A Request for Quote to Working Silicon, with an appreciation of how activities and decisions made in one phase affects another. It will also enable your Customer Support Engineering staff to provide an effective and proactive support to your ASIC customer. Product Development Engineers can also benefit from useful insight. This course also provides a well-structured guideline to Business Managers to be used as a reference for the ASIC biz.

The course is structured into modules. Short interactive workshops within the course facilitate in making this an interesting, interactive learning experience. Participants will be exposed to issues cited from real industry experience.

This course will be delivered by a senior VLSI consultant with extensive industry experience in supporting & managing ASIC projects on a global scale.

## What You Will Learn

- Basics of ASIC Design Libraries, Design Flow
- Basics of Verification especially DFM/DFY
- Basics of Design for re-use and IPs, guidelines for Low Power design
- Insight into ASIC technology and market trends
- Overview of MPW/MRS
- Economics involved in ASIC development and Managing an ASIC Program with a broad understanding of various generic issues seen and tips on addressing them
- These in turn will enable you in
  - How to effectively communicate with your customers
  - How to effectively support your customers

## Who Should Attend

- General IC & ASIC Design Engineers (1 – 4 years experience)
- Customer Support Engineers
- Product Development Engineers
- Sales & Marketing Professionals

## Prerequisite

Basic engineering know how. 1-2 years experience in IC design/support is preferable.

## Course Methodology

This course is conducted in a seminar room. The course will include brief interactive workshops like sessions to encourage participation and facilitate learning. Each participant will receive a set of course material. There are no lab sessions.

## Course Duration

3.5 - 4 days, 9.00 am – 5.00 pm

## Course Structure

*The course is organized into modules to facilitate participants to attend a specific module(s) as per their interest/need. To extract maximum benefit from the course however, participation in all modules is recommended.*

### A. Introduction to ASICs

- i. Standard cell based ASIC
- ii. Semi custom ASIC and Full custom ASIC
- iii. Brief outline of Design Flow
- iv. Brief outline of Library

### B. Design Library

- i. Definition
- ii. Library Architecture  
(With basic introduction to SSIs, IOs, Memories, IPs; general circuits used like Flip flops, latches, combinational circuits, RAMs, ROMs etc. will be included)
- iii. Library Cell Representations
- iv. Cell views (logical description, timing information, derating data, capacitance information, power and area information)
- v. Global views (max capacitance, interconnect info, max power and derating information)
- vi. Library Characterization  
Standard load, trip points, parasitic caps, input slew rate, timing equation (predicting delay), example of predicting delay
- vii. Library Validation
- viii. Trends in Library architecture  
Power, speed optimization, drive, contents changing with technology and trends

### C. Logic Simulation & Synthesis

- i. Simulation modes (behavioral, functional, static timing analysis, gate level simulation, transistor level simulation)
- ii. Net capacitance
- iii. Cell model (primitive, library, macro/IP), HDL Languages (Verilog, VHDL)
- iv. SDF in simulation
- v. Delay models (types of delays: pin to pin delay, input slope delay model)
- vi. Limitations of logic simulation
- vii. STA
- viii. Logic synthesis
- ix. Verilog and synthesis
- x. Handling Delays
- xi. Memory Synthesis
- xii. Timing driven synthesis
- xiii. RTL coding guidelines

### D. Floorplan, Placement & Routing, Finishing

- a. Floorplan
  - a. Goal, objective
  - b. I/O and Power planning
  - c. Core limited and pad limited design
  - d. Clock Planning

- b. Placement & Routing, Finishing
  - a. Goals & Objectives
  - b. Timing driven placement/Physical Design flow
  - c. Information formats
  - d. Routing
  - e. Global & detailed routing
  - f. Clock routing
  - g. Power Routing
  - h. Back Annotation
  - i. Circuit extraction
  - j. Design checks
  - k. Mask preparation

#### **E. Verification, DFT and DFM**

- i. Need
- ii. Functional Verification
  - a. Simulation
  - b. Formal Verification
  - c. Code coverage
  - d. Assertion Based Verification
- iii. Timing Verification
  - a. STA
  - b. SSTA
- iv. DFT
  - a. Scan
    - 1. Full scan
    - 2. Boundary scan
  - b. Faults – Fault models, Fault collapsing, IDDQ test, Fault simulation
  - c. ATPG
  - d. AT speed testing
  - e. BIST
  - f. Test logic insertion
- v. Physical Verification
  - a. DRC
  - b. LVS
  - c. Parasitic Extraction
- vi. Design for Manufacturability/Design For Yield (DFM/DFY)

#### **F. Design for Re-use & IPs**

- i. What is IP, what is Design Re-use
- ii. IPs (Driving factors, IP selection, IP verification, issues involved, generic portfolio)
- iii. Concurrently developed in-house IPs
- iv. Practical Design Re-use approach and essentials
- v. IP market landscape
- vi. Industry bodies

#### **G. Low Power Design Guidelines**

- i. Sources of power dissipation
- ii. Low power design techniques and methodologies  
(levels of low power optimization)
- iii. Low power design tools classification
- iv. Guidelines for low power design

## H. ASIC construction & Managing an ASIC program

- i. Basic economics involved in ASIC development
- ii. ASIC Program Flow
- iii. Key factors to be considered at ASIC start up
- iv. Selecting technology, library, IPs, package etc.
- v. Die size estimation, power estimation
- vi. Design interfaces
- vii. What is an ASIC program
- viii. Different functions
- ix. Documentation, check lists, sign-offs
- x. Issues seen during ASIC implementation
- xi. Guidelines for effective ASIC program management

## I. Multi Project Wafer Service/Multi Reticle Service

- i. What is MPW
- ii. When to/Why/Who goes for MPW
- iii. Generic MPW Flow model
- iv. What is Multi Reticle Service
- v. Foundry Perspective  
(Project Scheduling, Capacity Planning, General Pricing considerations)

## J. Trends in the ASIC arena

- i. Some definitions
- ii. Shift in ASIC technology & the underlying reasons
- iii. Insight into Structured ASICs/Platform ASICs
  - a. IPs used in Platform ASIC
  - b. Cell based ASIC vs. Platform ASIC
  - c. Some Industry examples illustrating the trend

### **Course Instructor**

*Meenu Sarin*

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**Mrs. Meenu Sarin** is a microelectronics professional with around 20 years experience in the microelectronics industry across various facets of operations & across geographies like Europe, India, Singapore, Greater China and Australia and with special focus in the semi custom ASIC environment. She has registered her company, VLSI Consultancy, in Singapore from where she works as a free-lance consultant. She has conducted in-house training courses and public workshops in various countries including Singapore, Malaysia, Hong Kong and India besides delivering talks in universities. She is also a founding member and an Executive Board Member of the Semiconductor Association, Singapore ([www.midas.org.sg](http://www.midas.org.sg))

From 1997-2002, Meenu was a Technical Marketing Manager in STMicroelectronics (STM)/Singapore with focus on Telecom segment. In this role, she was responsible for Business Development and Program Management for STM's semi custom ASIC projects in Asia Pacific. Meenu also worked as a Program Manager in charge of managing various semi custom projects with customers in the Asia-Pacific Region. Before her move to STM Singapore, Meenu worked at STM India from 1991 to 1997. As a Design Manager for Library Design Group, she was responsible for managing a 30 member team involved in design and development of semi custom digital libraries in various technologies across different platforms as per the market requirements and to support designers in STM's world wide locations. Prior to this, Meenu had been a Design Engineer for digital library design and development at STM Italy for several years after she received her engineering degree (Computer Engineering) from Delhi Institute of Technology, India in 1988.