VLSI Design Essentials

Synopsis

This course is aimed to provide an opportunity for the participant to acquire comprehensive technical and business insight into the VLSI Design arena.

VLSI Design is a complex process. This course provides a basic understanding & a holistic view of the complete IC design chain. It will enable your Design Engineer to understand the basics involved in various phases of IC design with an appreciation of how activities and decisions made in one phase affects another. It will also enable your Customer Support Engineering staff to provide an effective and proactive support to your customer. This course also provides a well-structured guideline to Business Managers & Program Managers to be used as a reference for the IC biz.

The course is structured into modules. Short interactive workshops within the course facilitate in making this an interesting, interactive learning experience. Participants will be exposed to issues cited from real industry experience. This course will be delivered by a senior VLSI consultant with extensive exposure in supporting & managing IC projects on a global scale.

What You Will Learn

- Basics of IC Design Libraries, IC Design Flow
- Basics of Verification especially DFM/DFY
- Basics of Design for re-use and IPs, guidelines for low power design
- Overview of MPW/MRS, Economics involved in IC development with a broad understanding of various generic issues seen and tips on addressing them
- These in turn will enable you to effectively communicate with & support your customers

Who Should Attend

- IC Design Engineers, Product Development Engineers (1- 4 years experience)
- Customer Support Engineers, Business Development Engineers, Program Managers

Prerequisite

Basic engineering know how. 1-2 years experience in IC design/support is preferable.

Course Methodology

This course is conducted in a seminar room. The course will include brief interactive workshops like sessions to encourage participation and facilitate learning. Each participant will receive a set of course material. There are no lab sessions.

Course Duration

3.5 days (9am – 5.00 pm)

Course Instructor

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Mrs. Meenu Sarin is a microelectronics professional with around 20 years' experience in the microelectronics industry across various facets of operations & across geographies like Europe, India, Singapore, Greater China and Australia and with special focus in the semi custom ASIC environment. She has registered her company, VLSI Consultancy, in Singapore from where she works as a free-lance consultant. She has conducted in-house training courses and public workshops in various countries including Singapore, Malaysia, Hongkong and India besides delivering talks in universities. She is also a founding member and an Executive Board Member of the Semiconductor Association, Singapore (www.midas.org.sg)

From 1997-2002, Meenu was a Technical Marketing Manager in STMicroelectronics (STM)/Singapore with focus on Telecom segment. In this role, she was responsible for Business Development and Program Management for STM's semicustom ASIC projects in Asia Pacific. Meenu also worked as a Program Manager in charge of managing various semi custom projects with customers in the Asia-Pacific Region. Before her move to STM Singapore, Meenu worked at STM India from 1991 to 1997. As a Design Manager for Library Design Group, she was responsible for managing a 30 member team involved in design and development of semi custom digital libraries in various technologies across different platforms as per the market requirements and to support designers in STM's world wide locations. Prior to this, Meenu had been a Design Engineer for digital library design and development at STM Italy for several years after she received her engineering degree (Computer Engineering) from Delhi Institute of Technology, India in 1988.

Course Structure

The course is organized into modules to facilitate participants to attend a specific module(s) as per their interest/need. To extract maximum benefit from the course however, participation in all modules is recommended.

A. Introduction

i. Basics of IC Design Flow
ii. Some definitions
iii. Generic Technology Aspects & Trends

B. Design Library

i. Definition
ii. Library Architecture
(with basic introduction to SSIs, IOs, Memories, IPs; general circuits used like Flip flops, latches, combinational circuits, RAMs, ROMs etc. will be included)
iii. Library Cell Representations
iv. Cell views (logical description, timing information, derating data, capacitance information, power and area information)
v. Global views (max capacitance, interconnect info, max power and derating information)
vi. Library Characterization
Standard load, trip points, parasitic caps, input slew rate, timing equation (predicting delay), example of predicting delay
vii. Library Validation
viii. Trends in Library architecture
Power, speed optimization, drive, contents changing with technology and trends

C. Logic Simulation & Synthesis

i. Simulation modes (behavioral, functional, static timing analysis, gate level simulation, transistor level simulation)
ii. Net capacitance
iii. Cell model (primitive, library, macro/IP)
iv. SDF in simulation
v. Delay models (types of delays: pin to pin delay, input slope delay model)
vi. Limitations of logic simulation
vii. STA
viii. Logic synthesis
ix. Verilog and synthesis
x. Handling Delays
xi. Memory Synthesis
xii. Timing driven synthesis
xiii. RTL coding guidelines

D. Floorplan, Placement & Routing, Finishing

a. Floorplan
    a. Goal, objective
    b. I/O and Power planning
    c. Core limited and pad limited design
    d. Clock Planning

b. Placement & Routing, Finishing
   a. Goals & Objectives
   b. Timing driven placement/Physical Design flow
   c. Information formats
   d. Routing
   e. Global & detailed routing
   f. Clock routing
   g. Power Routing
   h. Back Annotation
   i. Circuit extraction
   j. Design checks
   k. Mask preparation

E. Verification, DFT & DFM

i. Need
ii. Functional Verification
   a. Simulation
   b. Formal Verification
   c. Code coverage
   d. Assertion Based Verification
iii. Timing Verification
iv. DFT
   a. Scan
      1. Full scan
      2. Boundary scan
   b. Faults – Fault models, Fault collapsing, IDDQ test, Fault simulation
   c. ATPG
   d. At speed test
   e. BIST
   f. Test logic insertion
v. Physical Verification
   a. DRC
   b. LVS
   c. Parasitic Extraction
vi. Design For Manufacturability/Design For Yield (DFM/DFY)

F. Design for Re-use & IPs

i. What is IP, what is Design Re-use
ii. IPs (Driving factors, IP selection, IP verification, issues involved, generic portfolio)
iii. Concurrently developed in-house IPs
iv. Practical Design Re-use approach and essentials
v. IP market landscape
vi. Industry bodies

G. Low Power Design Guidelines

i. Sources of power dissipation
ii. Low power design techniques and methodologies (levels of low power optimization)
iii. Low power design tools classification
iv. Guidelines for low power design

H. Multi Project Wafer Service/Multi Reticle Service

i. What is MPW
ii. When to/Why/Who goes for MPW
iii. Generic MPW Flow model
iv. What is Multi Reticle Service
v. Foundry Perspective (Project Scheduling, Capacity Planning, General Pricing considerations)

I. Economics involved and some Generics

i. Basic Economics involved in IC development
ii. Generic issues seen during IC implementation